C. Amendments to the Claims.

1. (Currently Amended) A memory cell, comprising:

a first node for storing a first potential;

a second node for storing a second potential;

transistor gates formed from a gate layer; and

a capacitor having plates coupled between the first node and second node, a portion of ~~at least~~ one plate of the capacitor comprising a first interconnect wiring formed over the gate layer ~~and~~**that** includes a plurality of conductive layers **and** that **electrically** interconnects circuit ~~components~~**devices** of the memory cell.

2. (Original) The memory cell of claim 1, further comprising:

a first inverter having an input coupled to the first node and an output coupled to the second node; and

a second inverter having an input coupled to the second node and an output coupled to the first node; wherein

the first node stores a true data value and the second node stores a complementary data value.

3. (Original) The memory cell of claim 1, further including:

a first access transistor coupled to the first node; and

a second access transistor coupled to the second node.

4. (Cancelled)

5. (Currently Amended) The memory cell of claim 1, wherein:

the first ~~conductive~~ interconnect wiring includes a **plurality of separate portions, each portion including** bottom conductive layer, a dielectric layer formed over the bottom conductive layer, and a top conductive layer formed over the dielectric layer, the top conductive layer forming at least a portion of ~~the~~**a** first plate of the capacitor.

6. (**Currently Amended**) The memory cell of claim ~~4~~**5**, further including:

a second conductive interconnect wiring formed over the first conductive interconnect wiring that forms at least a portion of a second plate of the capacitor.

7. (Original) The memory cell of claim 6, wherein:

the second conductive interconnect wiring comprises titanium;

the bottom conductive layer comprises titanium nitride; and

the top conductive layer comprises titanium.

Claims 8 to 20 (Cancelled)

21. (**New**) The memory cell of claim 1, wherein:

the gate layer is not in physical contact with a drain of any transistor of the memory cell.

22. (**New**) The memory cell of claim 1, wherein:

a first portion of the first interconnect wiring is in physical contact with the drains of a first and second transistor of the memory cell; and

a second portion of the first interconnect wiring, separate from the first portion, is in physical contact with the drains of third and fourth transistor of the memory cell.

23. (**New**) A memory cell, comprising:

a first data storage node;

a second data storage node; and

a capacitor comprising a first plate coupled to the first data storage node, a second plate coupled to the second data storage node, and a third plate separated from the first and second plates by a capacitor dielectric, the first and second plates comprising portions of a interconnect

layer that electrically connects terminals of transistors of the memory cell to one another.